IN THE CLAIMS:

Please AMEND the claims as indicated below:

1. (CURRENTLY AMENDED) A semiconductor package obtained by collectively fabricating a plurality of semiconductor packages on a wafer in a batch process producing a wafer product and dicing the wafer product into discrete semiconductor packages, wherein:

said semiconductor package is a stacked body formed by bonding two or more semiconductor devices through an insulating layer;

each of said semiconductor devices comprises a substrate and a device pattern formed on a surface thereof; and

a device pattern surface of a lower semiconductor device faces a non-device pattern surface of a semiconductor device stacked on said lower semiconductor device, wherein

said semiconductor device positioned, in sequence, as a lowermost ~~layers~~ semiconductor device ~~further comprises~~ and further comprising a back surface protective film, and a heat radiation layer, of a material having a high heat transfer rate, on the non-device pattern surface of the ~~wafer~~ lowermost semiconductor device, and

said back surface protective film is bonded to a back surface of the stacked body by bonding an epoxy resin film to form the back surface protective film.

2. (CANCELLED)

3. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is deposited on the non-device pattern surface of a wafer as the lowermost layer, before said semiconductor packages are diced.

4. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is one formed by a thin film formation technology.

5. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer is made of copper, aluminum or an alloy.

6. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said heat radiation layer also acts as a support.

7. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said insulating layer comprises a polyimide resin or an epoxy resin.

8. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein said semiconductor device positioned as the uppermost layer further comprises a resin sealing layer on the device pattern surface thereof, and said resin sealing layer is one formed on the device pattern surface of the wafer as the uppermost layer, before said semiconductor package is diced.

9. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 1, wherein the device patterns of said semiconductor devices stacked are electrically connected to one another through a re-wiring layer and a substrate through-electrode that are simultaneously formed in one semiconductor device.

10. (PREVIOUSLY PRESENTED) The semiconductor package as defined in claim 9, wherein each of said re-wiring layer and said substrate through-electrode is formed of copper or its alloy.

11. (CANCELLED)

12. (CANCELLED)

13. (CANCELLED)

14. (CANCELLED)

15. (CANCELLED)

16. (CANCELLED)

17. (CANCELLED)

18. (CANCELLED)